ABSTRACT

A method for forming selective P type and N type gates is described. A first gate oxide layer is grown overlying a semiconductor substrate. A polysilicon layer is deposited overlying the first gate oxide layer. The polysilicon layer is patterned to form first NMOS gates. A second gate oxide layer is grown overlying the substrate. A polysilicon-germanium layer is deposited overlying the second gate oxide layer and the first gates. The polysilicon-germanium layer and first gates are planarized to a uniform thickness. The polysilicon first gates and the polysilicon-germanium layer are patterned to form second NMOS polysilicon gates and PMOS polysilicon-germanium gates.